

Major top level details of chip/block - please provide salient data wherever possible

- Clock frequency
- Die area targeted- mm X mm
- Choice of technology
- Packaging type suggested
- Feature size of design
Minimum Gate length in microns
- Number of Input pins
- Number of output pins
- Number of I/O pins
- Number of power pins
- Estimated power budget
- Name of foundry selected / options

- | | | | |
|---|---------------------------------|----------------------------------|---|
| <input type="checkbox"/> Manufacturing Process name | <input type="checkbox"/> SOI | <input type="checkbox"/> BCDCMOS | <input type="checkbox"/> Bipolar |
| | <input type="checkbox"/> BiCMOS | <input type="checkbox"/> CMOS | <input type="checkbox"/> Other- specify |