

## General Description

The current steering DAC is used for the realization of Nyquist rate DACs, which means the DAC operate on data samples generated their outputs at the sampling frequency. A major advantage of current steering DAC architecture is its inherent high current drive and high speed. Appropriate number of binary weighted reference currents is used to create the DAC output current in the binary weighted implementation of current steering DAC.

Another uses thermometer codes to switch current is called thermometer decoded implementation. Binary weighted implementation requires small silicon area but has large DNL and dynamic error. Thermometer decoded implementation has low DNL error, guaranteed monotonicity and reduce glitching noise, but increased complexity, area and power consumption of the thermometer decoder. To get the best of both worlds, this 10 bit current steering DAC are implemented using segmented architecture, i.e. 4 binary and 6 unary bits

## Features

- Resolution: 10 Bit
- Differential Non-Linearity (DNL): < 0.5 LSB
- Peak to Peak Output Range: 1.2V (@VDD = 3V)
- Signal to Noise Ratio: > 50 dB
- Integral Non-Linearity (INL): < 1.0 LSB
- Conversion Rate: 30 MHz
- Power Consumption : < 10mW
- Process Technology: 0.13um

## Block Diagram

