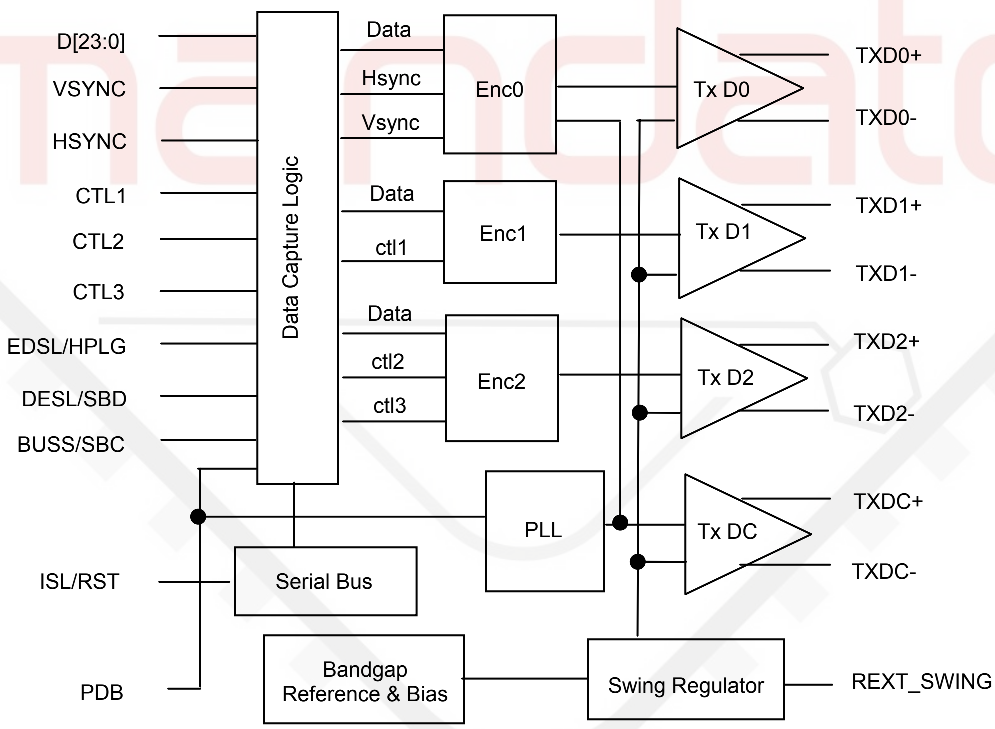
General Description

The DVI transmitter support displays ranging from VGA to UXGA resolutions (25MHz-165MHz) using a single link interface. The DVI transmitter has a highly flexible interface with either a 12-bit mode (½ pixels per clock edge) or 24-bit mode 1-pixel/clock input for true color (16.7 million) support. In 24-bit mode, the DVI transmitter supports single or dual edge clocking. In 12-bit mode, the DVI transmitter supports dual edge single clocking or single edge dual clocking. The DVI transmitter support Receiver and Hot Plug Detection.

Features

- Scaleable Bandwidth: 25MHz-165MHz (VGA to UXGA)
- Support Dual-Link operation up to 330Mbps
- Integrated High-bandwidth Content protection (HDCP)
- Flexible Graphics Controller Interface: 12-bit (½ pixel) or 24-bit mode 1 pixel/clock inputs
- Flexible Input Clocking: Single clock single edge (24-bit), Single clock dual edge (12-/24-bit), Dual clock single edge (12-bit)
- Low Voltage Interface: 3.3V
- Serial Bus Slave Programming interface
- Receiver Detection: Supports Hot Plug Detection
- Standards Compliant with DVI 1.0 (DVI is backwards compliant with VESA, P&D, TM and DFP

Block Diagram



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I/O Pad Description

Pad Name	Pad No	Type	Description
BSEL/SCK		Input	**Bus Select / Serial Bus Clock**. This pin is an open collector input. If SERIAL BUS is enable (ISL = HIGH), then this pin is the SERIAL BUS clock input. If the SERIAL BUS is disabled (ISL = LOW), then this pin selects the input width (12/24 bits). **HIGH** selects 24-bit input mode, **LOW** selects 12-bit input mode. *Note: When RSV pin is tired HIGH and PDB is LOW, the chip works in scan mode for digital logic test. In this mode, BSEL pin is used as clock 1 input.*
DESL/SDA	(open drain o/p)		**Dual edge clock select / SERIAL BUS Data**. This pin is an open collector input. If SERIAL BUS bus is enabled (ISL = HIGH), then this pin is the SERIAL BUS data I/O line. If the SERIAL BUS bus is disabled (ISL = LOW), then this pin determines whether dual/single edge clocking is used. **Dual edge clock select:** When DESL=HIGH, IDCLK+ latches input data on both falling and rising clock edges. When DESL=LOW, IDCLK+/IDCLK- latches input data on only falling or rising clock edges. See the differences between 12 and 24 bit below **In 12-bit mode (BSEL = LOW)**: If HIGH (dual edge), IDCLK+ is used to latch data on both falling and rising edges. If LOW (single edge), IDCLK+ latches 1st half data and IDCLK- latches 2nd half data. **In 24-bit mode (BSEL = HIGH):** DESL must be set LOW *Note: When RSV pin is tired HIGH and PDB is LOW, the chip works in scan mode for digital logic test. In this mode, DESL pin is used as clock 0 input.*
EDGE/CHG		Input	**Edge select / Monitor Charge**. If the SERIAL BUS is enabled (ISL = HIGH), then this input pin is as monitor detect signal. NOTE: This is a 3.3V tolerant input without hysteresis. If SERIAL BUS is disabled (ISL = LOW), then this pin selects the latch edge. The edge setting function depends on whether dual or single edge data latching is selected: **Dual Edge Mode** (DESL = HIGH) EDSL = LOW, the primary edge (first. even latch edge after DE is asserted) is falling edge. EDSL = HIGH, the primary edge (first odd latch edge after DE is asserted) is the rising edge. NOTE: In dual edge mode, the control signals HS and VS are only latched on the secondary clock edge. **Single Edge mode** (DESL = LOW) EDSL = LOW, the falling edge of the clock is used to latch data. EDSL = HIGH, the rising edge of the clock is used to latch data. *Note: When RSV pin is tired HIGH and PDB is LOW, the chip works in scan mode for digital logic test. In this mode, EDGE pin is used as SCAN input.*
PDB		Input	**Power Down** (active low). A High level indicates normal operation and a Low Level indicates power down mode. During power down mode, digital input, output buffers and SERIAL BUS interface are NOT disabled. The DVI transmitter's digital Core is powered down. *Note that when ISL = HIGH, this pin should be tied LOW to ensure the*

			chip is powered off when reset is asserted. *Note: See RSV pin for test mode configuration.*
VREF	Analog		**Input Reference Voltage**. Selects the swing range of the digital parallel data inputs (D23:0], DE. VSYNC, HSYNC, and IDCK)
EXT_RES	Analog		**Voltage Swing Adjust**. A resistor should tie this pin to AVDD. The amplitude of the voltage swing is determined by the value of this resistance. For remote display applications, 400W is recommended. For notebook computers, 680W is recommended.
MSEN	O (Open Drain)	Input	**Monitor Sense**. This output is programmable through the SERIAL BUS interface as follows: 000 – Force MSEN output high (disabled); 001 – Outputs the MDI bit (interrupt bit) 010 – Output the RCVS bit (receiver detect) 011 – Output the HPLG bit (hot plug detect) Note: An external 5k pull-up resistor to VDD is required at this pin for proper operation.
DK2/MDA, DK1/MCL		I/O	**Multi-function input.** When I2C is disable, they are used to select the de-skew setting for the data & clock input bus. When I2C is enabled, DK2 & DK1 are used for I2C interface for EEPROM access as indicated by the pin name. *Note: This two pin require a pull-up resistor (1K suggested) when used for I2C interface.*
DK3		I/O	When I2C is disable, they are used to select the de-skew setting for the data & clock input bus. *Note: When RSV pin is tired HIGH and PDB is LOW, the chip works in scan mode for digital logic test. In this mode, DK3 pin is used as SCAN Enable.*
TXD0+	Analog		Low Voltage Differential Signal output data pair **(BLUE)**, DVI 1.0 compliant
TXD0-	Analog		
TXD1+	Analog		Low Voltage Differential Signal output data pair **(GREEN)**, DVI 1.0 compliant
TXD1-	Analog		
TXD2+	Analog		Low Voltage Differential Signal output data pair **(RED)**, DVI 1.0 compliant
TXD2-	Analog		
TXC+	Analog		Low Voltage Differential clock output data pair, DVI 1.0 compliant
TXC+	Analog		
VDD	Power		**Digital Core VDD**, nominally 3.3.V.
GND	Ground		**Digital ground**
ADD	Power		**Analog VDD**, nominally 3.3.V.
AGND	Ground		**Analog ground**
HSYNC	Digital	Input	**Horizontal Sync**
VSYNC	Digital	Input	**Vertical Sync**
D[23:15]	Digital	Input	**Upper 9-bits of 24-bit pixels data bus.** *Note: When BSEL is set LOW, these bits are not used to input pixel data. In this mode, the bit D[23:16] are the source data of I2C register CFG. This allows host to read the configuration data of the graphic card chip which is connected to the transmitter through the transmitter's I2C interface.*
D14/SYNCO	Digital	I/O	Part of the 24-bit pixel bus, when BSEL is set HIGH; When BSEL is LOW, this pin is used as SYNC output in Dual-Link mode.

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<table>
<tr><td>D13/MAST,
D12/DUAL</td><td>Digital</td><td>I/O</td><td>Part of the 24-bit pixel bus, when BSEL is set HIGH;
When BSEL is LOW, this pin is used together with DUAL for mode configuration as follows:
<table><tr><th>[DUAL, MAST]</th><th>Mode</th></tr><tr><td>00</td><td>Single-Link</td></tr><tr><td>01</td><td>Reserved</td></tr><tr><td>10</td><td>Dual-Link Slave</td></tr><tr><td>11</td><td>Dual-Link Master</td></tr></table></td></tr>
<tr><td>D[11:0]</td><td>Digital</td><td>Input</td><td>Lower 12 bits of 24-bit pixel bus.</td></tr>
<tr><td>IDCLK+</td><td></td><td></td><td>Input Data Clock +
Positive edge clock used for both 24/12 bit modes</td></tr>
<tr><td>RSV</td><td></td><td>Input</td><td>It must be tied to LOW in normal operation mode.
When it is tied to HIGH, the chip works in test mode. The mode is configured together with PD pin as follows:
<table><tr><th>[RSV, PD]</th><th>Mode</th></tr><tr><td>00</td><td>Power-Down</td></tr><tr><td>01</td><td>Normal Operation</td></tr><tr><td>10</td><td>Scan Mode for Digital Blocks</td></tr><tr><td>11</td><td>Analog Test</td></tr></table></td></tr>
<tr><td>IDCLK-</td><td></td><td></td><td>Input Data Clock –
This clock is only used in 12-bit mode when dual edge clocking is not used (DESL = LOW). It provides the odd latching edges for single edge dual clock mode. If BSEL = HIGH or if DESL = HIGH this pin is not used and should be tied to VSS/GND.</td></tr>
<tr><td>ISL/RST</td><td>Digital</td><td>Input</td><td>Serial Bus Interface Select. If HIGH, the Serial Bus interface is active. If low, the serial bus is not active and the chip is hardware programmed through the configuration pins. This pin also acts as an asynchronous reset to the serial bus interface controller. The reset is active when this input is held LOW.</td></tr>
</table>

I^{2}C Slave Interface & Register Configuration

I2C Serial Bus interface and I2C register set are implemented in this block to allow chip configuration by firmware for programmability. The I2C slave state machine does not require an internal clock and support only byte read and write. Page mode is not supported.

The basic access cycle consists of the following phases:
A start condition (HIGH to LOW transition of SDA while SCL is HIGH)
A slave address phase (Slave Device Address: 0111000X, where X is Read/Write bit: 1 - Read, 0 - Write)
A sub-address phase (8 Bits, Register Address)
A data phase (8 Bits, Read/Write Data)
A stop condition (LOW to HIGH transition of SDA while SCL is HIGH)

I^{2}C Write Cycle:

<table>
<tr><td rowspan="2">S</td><td colspan="8">Slave Address</td><td rowspan="2">A</td><td>Sub-Address</td><td rowspan="2">A</td><td>Data</td><td rowspan="2">A</td><td rowspan="2">P</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>W</td><td>SADDR[7:0]</td><td>DAT[7:0]</td></tr>
</table>

I^{2}C Read Cycle:

<table>
<tr><td rowspan="2">S</td><td colspan="8">Slave Address</td><td>A</td><td>Sub-Address</td><td>A</td><td>P</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>W</td><td></td><td>SADDR[7:0]</td><td></td><td></td></tr>
</table>

S	Slave Address	A	Data	A	P

	0	1	1	1	0	0	0	R		DAT[7:0]		

Register Mapping

Register Address	Register Name	Type	Register Bits							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0
0x0	VEN_IDL	R	Vendor ID register – Low Byte							
0x1	VEN_IDH	R	Vendor ID register – High Byte							
0x2	DEV_IDL	R	Device ID register – Low Byte							
0x3	DEV_IDH	R	Device ID register – High Byte							
0x4	DEV_REV	R								
0x5	Reserved	R								
0x6	FRQ_L	R								
0x7	FRQ_H	R								
0x8	CONFIG		Reserved		VEN	HEN	DSEL	BSEL	EDGE	PD
0x9	RSENCTRL		VLOW	MSEL [2:0]			TSEL	RSEN	HTPLG	MDI
0xA	DK_CTL		DK [3:1]			DKEN	CTL [2:1]			Reserved
0xB	CFG		CFG [7:0]							
0xC			SCNT	DUAL	MAST	PLLF [3:0]				PFEN
0xD			DCTL [2:0]			Reserved				
0xE			Reserved							
0xF			Reserved	ENC_ON	BKSV_ERR	RX_RPTR	TX_ANSTOP	CP_RESETN	RI_RDY	ENC_EN
0x10~0x14	WR_BKSV	WO	5-Bytes BKSV							
0x15~0x1C	WR_AN	RW	8-Bytes AN							
0x1D~0x21	AKSV	RO	5-Bytes AKSV							
0x22	RI_1	RO	RI_1 [7:0]							
0x23	RI_2	RO	RI_2 [7:0]							
0x33	VHS_POL				V_POL	H_POL				

Register Bit Definition

VEN_ID (0x00, 0x01)

7	6	5	4	3	2	1	0
VEN_ID[7:0]							
7	6	5	4	3	2	1	0
VEN_ID[15:8]							

This register contains 16 bit vendor ID. VEN_ID [15:0] is hardwired to 0xXXXX.

DEV_ID (Address: 0x02, 0x03, Read Only; Default: 0x011A)

7	6	5	4	3	2	1	0

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VEN_ID[7:0]							
7	6	5	4	3	2	1	0
VEN_ID[15:8]							

This register contains 16 bit FTD Device ID. DEV_ID [15:0] is hardwired to 0x011A.

DEV_REV (Address: 0x04; Read Only; Default: 0x01)

7	6	5	4	3	2	1	0
VEN_ID[15:8]							

This register contains the revision ID. REV_ID [7:0] is hardwired to 0x01

CONFIG (Address: 0x08; Read/Write; Default: 0x00)

7	6	5	4	3	2	1	0
Reserved		VEN	HEN	DESL	BSEL	EDSL	PDB

VEN Vertical Sync Enable
- 0 – HSYNC is transmitted as fixed low
- 1 - HSYNC is transmitted as is

HEN Horizontal Sync Enable
- 0 – VSYNC is transmitted as fixed low
- 1 - VSYNC is transmitted as is

DESL Dual Edge Clock Select;
- 0 – Input data is single edge latched;
- 1 - Input data is dual edge latched.

BSEL Input Bus Select
- 0 - Input bus is 12 bits wide;
- 1 – Input bus is 24 bits wide.

EDSL Edge Select
- 0 – Input data is falling edge latched;
- 1 - Input data is rising edge latched.

PDB Power Down mode
- 0 – Power Down
- 1 – Normal Operation

RCVSCTRL (Address: 0x09; Read/Write; Default: 0x00)

7	6	5	4	3	2	1	0
VLOW(RO)	MONSL[2:0]			MDISL		HPLG	MDI

VLOW This bit is a read only bit and should be set to 1 by hardware if the VREF signal indicates low swing input; high swing input otherwise.

MONSL Select source of the MSEN output pin
- 000 – Force MSEN output high (disabled)
- 001 – Outputs the MDI bit (interrupt bit)
- 010 – Output the RCVS bit (receiver detect)
- 011 – Output the HPLG bit (hot plug detect)

MDISL Interrupt Generation Method
- 0 – Interrupt bit (MDI) is generated by monitoring RCVS
- 1 – Interrupt bit (MDI) is generated by monitoring HPLG

HPLG Hot Plug Detect input, the state of HPLG pin can be read from this bit.

MDI Monitor Detect Interrupt:
- 0 – Detection signal has changed logic level. Note: write one to this bit to clear.

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DK_CTL (Address: 0x0A; Read/Write; Default: 0x00)

7	6	5	4	3	2	1	0
DK[3:1]			DKEN	CTL[3:1]			Reserved

DK [3:1] DE-Skewing setting. Increment T psec:
000: 1 step – Minimum setup/Maximum hold
001: 2 step
010: 3 step
011: 4 step
100: 5 step
101: 6 step
110: 7 step
111: 8 step – Maximum setup/Minimum hold

CTL [3:1] General purpose input (same as CTL [3:1] pin input)

DKEN De-skewing enable through DK [3:1] bits. HIGH when enabled, LOW otherwise.

CFG (Address: 0x0B; Read Only; Default: 0x00)

7	6	5	4	3	2	1	0
CFG[7:0]							

This read only register contains state of inputs D23:16]. These pins can be used to provide user selectable configuration data though the I2C bus. Note: it is only available in 12 bit mode.

VHS_POL (Address: 0x33; Rea/Write; Default: 0x00)

7	6	5	4	3	2	1	0
Reserved		VS_POL	HS_POL	Reserved			

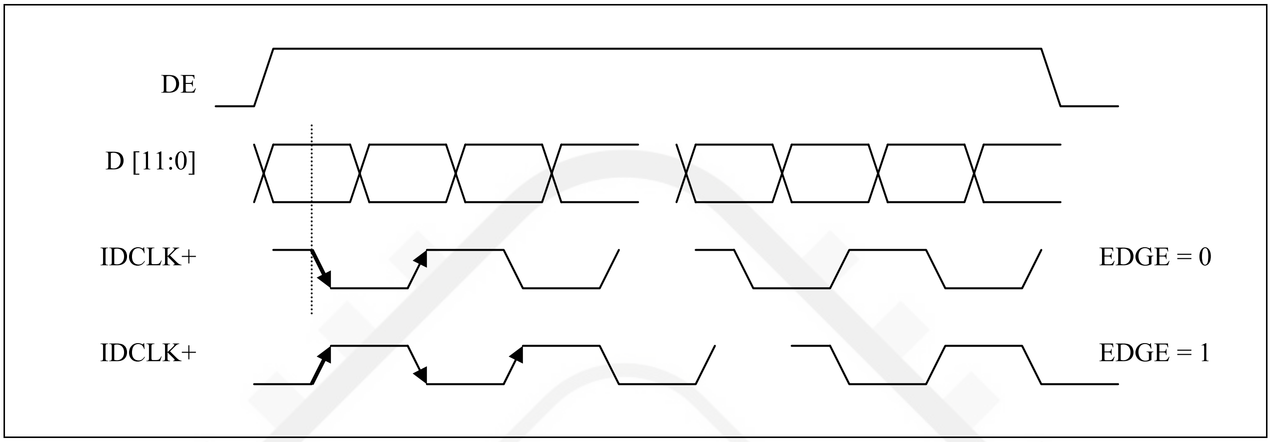
These two bits allows chip configurable to any polarity of VSYNC and HSYNC for different applications. They are defined as follows:

VHS_POL[5:4]	Description
00	Positive Polarity (Leading edge rises) for both VSYNC and HSYNC
01	Positive Polarity (Leading edge rises) for VSYNC and Negative Polarity (Leading edge falls) for HSYNC
10	Negative Polarity (Leading edge falls) for VSYNC and Positive Polarity (Leading edge rises) for HSYNC
11	Negative Polarity (Leading edge falls) for both VSYNC and HSYNC

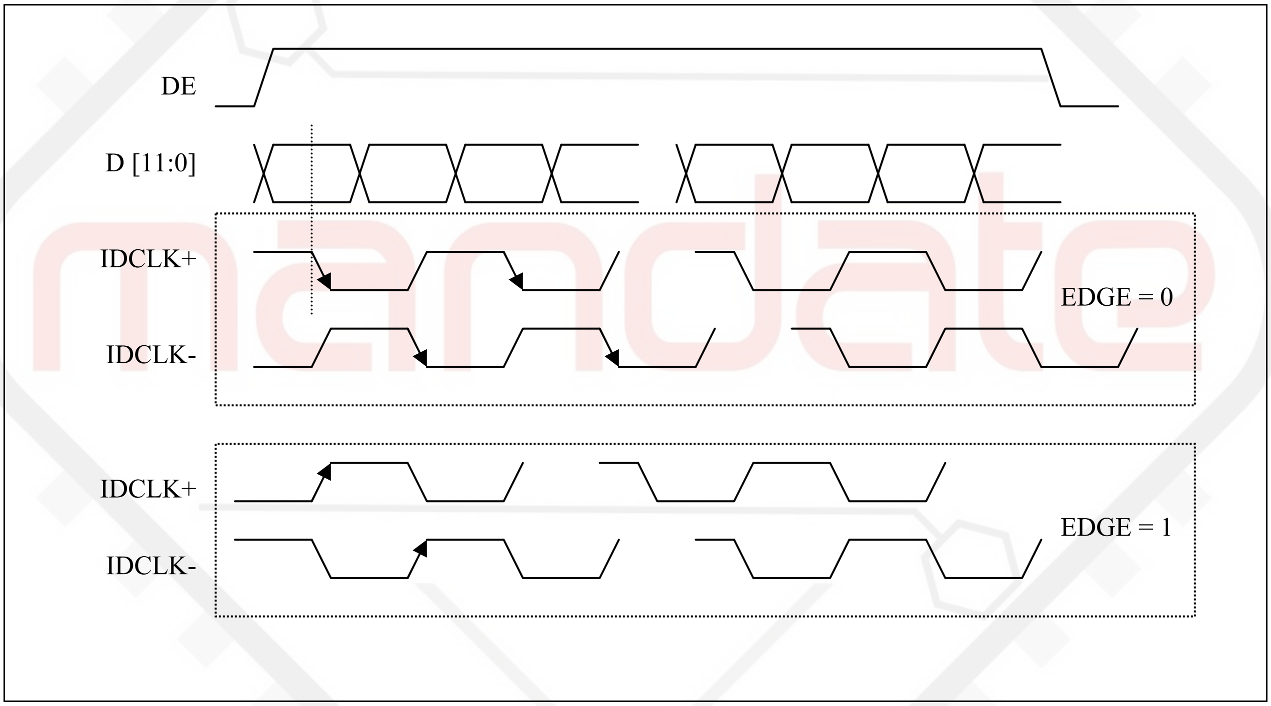
<u>12-Bit Mode (BSEL = 0)</u>

In 12-bit mode, the data latch supports dual edge single clocking and single edge dual clocking as shown in Figure XX

Dual Edge Single Clocking (BSEL = 0; DSEL = 1):



Single Edge Dual Clocking (BSEL = 0; DSEL = 1):

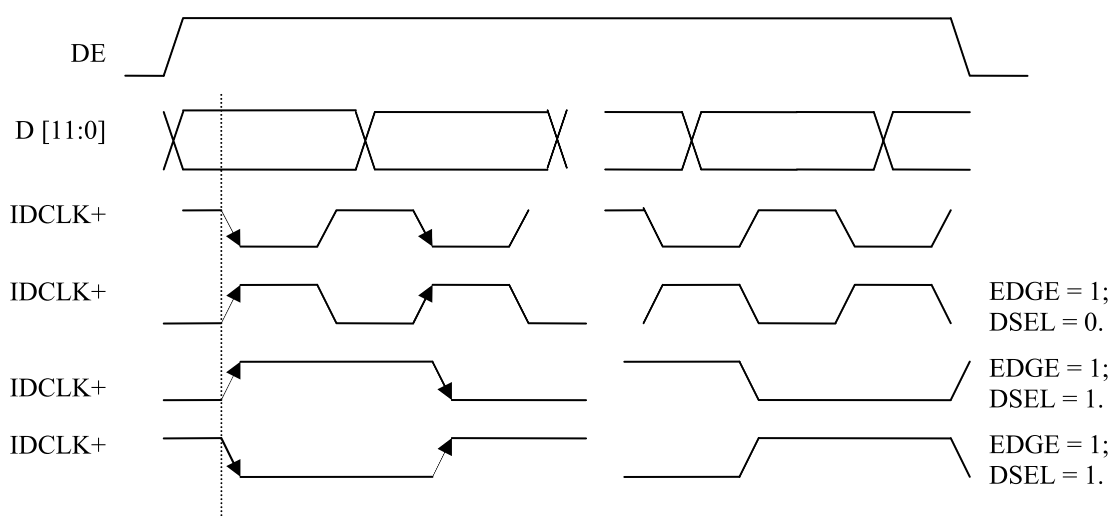


Pin Name	P0-L	P0-H	P1-L	P1-H	P2-L	P2-H
D11	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]

D6	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

24-Bit Mode (BSEL = 1)

In 24-bit mode, the DVI transmitter uses only one clock IDCLK+ and supports single and dual edge clocking.



Data Mapping

Pin Name	P0	P1	P2
D23	R0[7]	R1[7]	R2[7]
D22	R0[6]	R1[6]	R2[6]
D21	R0[5]	R1[5]	R2[5]
D20	R0[4]	R1[4]	R2[4]
D19	R0[3]	R1[3]	R2[3]
D18	R0[2]	R1[2]	R2[2]
D17	R0[1]	R1[1]	R2[1]
D16	R0[0]	R1[0]	R2[0]
D15	G0[7]	G1[7]	G2[7]
D14	G0[6]	G1[6]	G2[6]
D13	G0[5]	G1[5]	G2[5]
D12	G0[4]	G1[4]	G2[4]
D11	G0[3]	G1[3]	G2[3]
D10	G0[2]	G1[2]	G2[2]
D9	G0[1]	G1[1]	G2[1]
D8	G0[0]	G1[0]	G2[0]
D7	B0[7]	B1[7]	G2[7]
D6	B0[6]	B1[6]	G2[6]
D5	B0[5]	B1[5]	G2[5]

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D4	B0[4]	B1[4]	G2[4]
D3	B0[3]	B1[3]	G2[3]
D2	B0[2]	B1[2]	G2[2]
D1	B0[1]	B1[1]	G2[1]
D0	B0[0]	B1[0]	G2[0]

Note: In 24-bit Single Clock Dual Edge mode, the Data Latch logic will look at the first clock edge (either falling or rising) after DE goes high to determine the first pixel data.

Input Data Timing Diagram

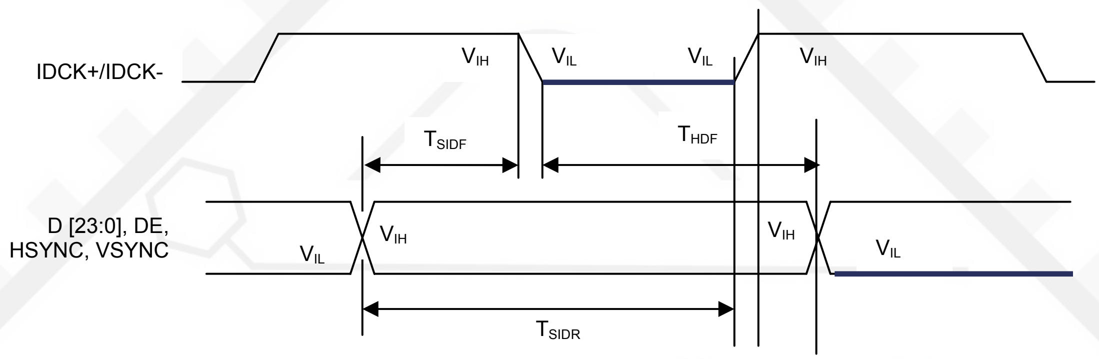

Figure 3. Control and Single-Edge-Data Set-up/ Hold Times to IDCK+/IDCK-

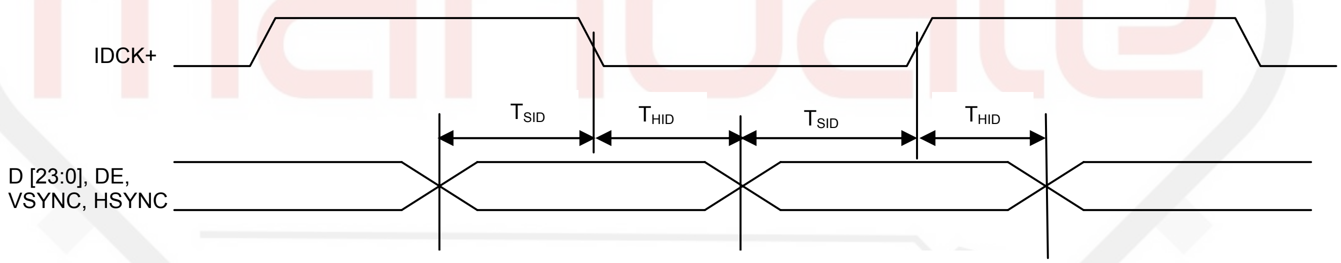

Figure 4. Dual Edge Data Setup/Hold Times to IDCK+

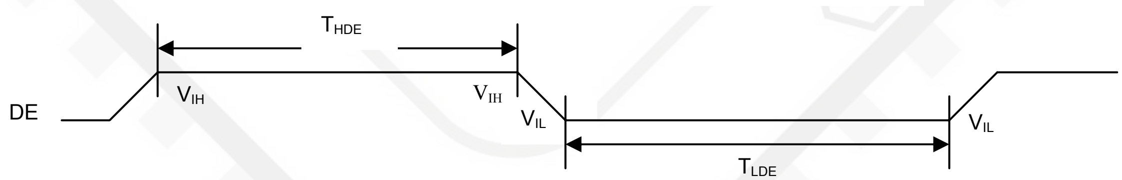

Figure 5. VSYNC, HSYNC Delay Times from/to DE

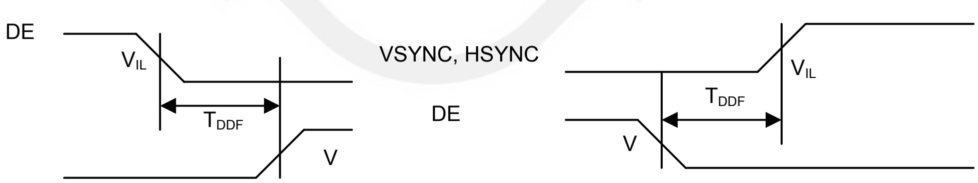

Figure 6. DE High/Low Times

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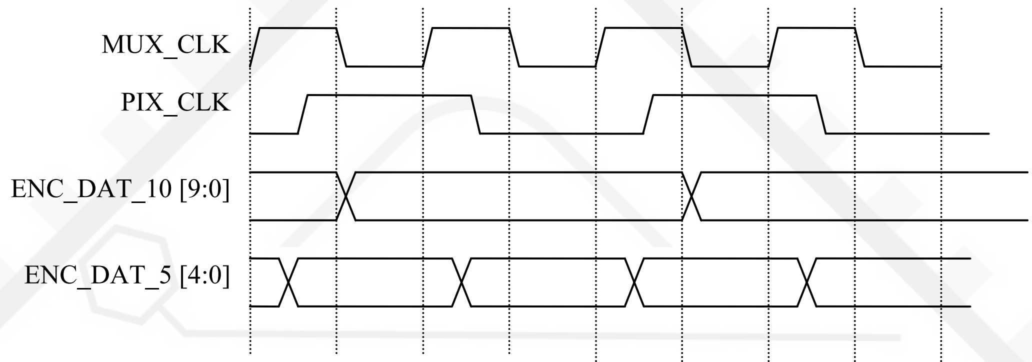
Output Bus Timing Diagram



HDCP-CIPHER

HDCP cipher engine produces all required values based on an associated set of key and KSV (Key Selection Vector):

- 64-bit Pseudorandom value An,
- 16-bit Synchronization Verification value R0 in Authentication phase and Ri during Vertical Blank period, and
- 24-bit wide key-dependent pseudo-random stream at every input clock during active pixel data.

Host may read these values through a set of registers described in register definition below.

The HDCP cipher consists of three major sub-modules, which are LFSR Module, Block Module and Output Function. Each of these modules is described in the High-Bandwidth Digital Content Protection System specification Revision 1.0. Please refer it for module design and firmware/test case development.

A state machine controls the sequence of the cipher operation in steps as follows:

1. *Load the B & K registers in Block Module with initial values K_{init} and B_{init}*
2. *Apply 48 clocks to the Block Module registers*
3. *Save the least significant 56 bits of the B register for future use as Ks at authentication and Ki at vertical blank*
4. *Transfer 84-bit B register values to the K registers*
5. *Reload B register with the same initial value Binit*
6. *Initialize the LFSR Module with Ks*
7. *Assert re-key enable*
8. *Apply 56 clocks to the LFSR and Block Modules, saving the 64-bit Mi value during the last four clocks*
9. *De-assert re-key enable.*

A 64-bit pseudo-random value, A_n, is generated by hardware with firmware control by clearing and then setting the 'TX_ANSTOP' bit of the 'CTRL_REG' register. At the assertion of 'AT_ANSTOP', A_n is written

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into the 'WR_AN_REG' register automatically by hardware. Assertion of 'TX_ANSTOP' also indicates the start of the authentication process.

K_m, the initial value used to initialize K register, is calculated on-fly while the key is fetched from an external E^2PROM (24LC32, its address is set at A6h) via I^2C interface. The key fetching is initiated by sending a one-clock-cycle pulse, 'KEY_LOAD_EN', to I^2C master once the register 'WR_BKSV_REG' is written.
Note that KSV must be read and put into register AKSV_REG by hardware prior to the key fetching by issuing a pulse, 'KSV_LOAD_EN' at the power-on.

Interface with I^2C master is illustrated in the Key-Loading Timing Diagram below. The Personality Byte, KSV and Keys are stored in the PROM as shown in table below. The Personality Byte is used to blank screen during authentication if set to 00h, i.e., ENC_RGB bus is forced to zero, or show screen if set to 01h, i.e., RGB_IN data bypasses during authentication.

PROM Memory Map

Address	Content
0x0000	Personality Byte
0x0001	KSV[0]
0x0002	KSV[1]
0x0003	KSV[2]
0x0004	KSV[3]
0x0005	KSV[4]
0x0006	Key00[0]
0x0007	Key00[1]
0x0008	Key00[2]
0x0009	Key00[3]
0x000A	Key00[4]
0x000B	Key00[5]
0x000C	Key00[6]
0x000D	Key01[0]
0x000E	Key01[1]
…	…
0x0145	Key39[7]

Register Definition

HDCP_CTRL (Address: 0x0F; Default: 0x00)

7	6	5	4	3	2	1	0
Reserved	ENC_ ON	BKSV_ER R	RX_ RPTR	TX_ ANSTOP	CP_ RESTN	RI_RDY	ENC_EN

This control register allows firmware to check the status and initiate the encryption according to the protocol.

Bit-7: Reserved;

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ENC_ON: This bit is read only. One indicates that the encryption is enabled and encryption is in process.

BKSV_ERR: Read Only. This bit is set by hardware when a BKSV value is written that does not have the proper structure. This bit is cleared when a valid BKSV value is written *or by hardware*.

RX_RPTR: This bit is set by firmware prior to authentication if the receiver is a repeater.

TX_ANSTOP: When this bit is cleared, the cipher engine is allowed to free-run and the WR_AN registers will cycle through a sequence of pseudo-random values. When this bit is set, cycling stops and the value in the WR_AN register is held and can be read by firmware to initiate the AN register in the receiver.

Note: This bit is automatically cleared under any of the following conditions:

- *Power-on Reset*
- *BKSV_ERR*
- *RX_RPTR is changed*

CP_RESTN: This is the soft-reset bit for cipher engine. This bit is asserted (active LOW – 0) only by hardware reset. It can be de-asserted (one) at any time.

RI_RDY: Read only. One indicates the first Ri value is available. This bit is cleared by power-on reset.

ENC_EN: Encryption Enable. When this bit is set, the transmitter encrypts all data. This bit can be only cleared by power-on reset.

WR_BKSV (Address: 0x10 ~ 0x14; Write Only; Default: 0x00)

7	6	5	4	3	2	1	0
WR_BKSV_1[7:0]							
WR_BKSV_2[7:0]							
WR_BKSV_3[7:0]							
WR_BKSV_4[7:0]							
WR_BKSV_5[7:0]							

These 5 bytes of register set allows firmware write 5 bytes of BKSV read from receiver. Byte 1 is the LSB, byte 5 is MSB. The byte 5 should be written last and then trigger the authentication process in this transmitter.

AKSV (Address: 0x1D ~ 0x21; Read Only; Default: 0x00)

7	6	5	4	3	2	1	0
AKSV_1[7:0]							
AKSV_2[7:0]							
AKSV_3[7:0]							
AKSV_4[7:0]							
AKSV_5[7:0]							

These 5-byte register set contains transmitter's KSV (key selection vector). The 40-bit KSV value together with 40 keys of 56-bits are stored in an external E2PROM. They are fetched by an integrated I2C master.

Note: All five bytes should be read from here and then written to the receiver. Byte 5 should be written last into the receiver, and will trigger the authentication process in the receiver.

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WR_AN (Address: 0x15 ~ 0x1C; Read/Write; Default: 0x00)

7	6	5	4	3	2	1	0
WR_AN_1[7:0]							
WR_AN_2[7:0]							
WR_AN_3[7:0]							
WR_AN_4[7:0]							
WR_AN_5[7:0]							
WR_AN_6[7:0]							
WR_AN_7[7:0]							
WR_AN_8[7:0]							

This 8-byte register set contains 64 bits pseudo-random value. The value can be read by firmware and used in the authentication process. Alternatively, this value can be generated by firmware or hardware (board), and then written into this register. Eight Bytes: Byte 1 is the LSB, Byte 8 is the MSB.

RI_12 (Address: 0x22 ~ 0x23; Read Only; Default: 0x00)

7	6	5	4	3	2	1	0
RI_1[7:0]							
RI_2[7:0]							

This 2-byte read only register contains the synchronization verification value Ri. It can be read by the host and compared against the Ri value read from the receiver to sure that the encryption process on the transmitter and receiver are synchronized.

Electrical Specifications

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	-0.3	3.3	4.0	V
V_I	Input Voltage	-0.3	-	VCC+0.3	V
V_o	Output Voltage	-0.3	-	VCC+0.3	V
T_A	Ambient Temperature (with power applied)	-25	-	105	° C
T_{STG}	Storage Temperature	-40	-	125	° C
P_{PD}	Package Power Dissipation	-	-	1	W

Notes: [1] Permanent device damage may occur if absolute maximum conditions exceeded.
[2] Functional operations should be restricted to the conditions under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise[1]	-	-	100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	° C

Notes: [1] Guaranteed by design.

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DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Swing High-level Input	$V_{REF} = V_{CC}$	2.0	-	-	V
V_{IL}	High Swing Low-level Input Voltage	$V_{REF} = V_{CC}$	-	-	0.8	V
V_{DDQ}[2]	Low Swing Voltage		1	-	1.8	V
V_{SH}	Low Swing Low-Level Input Voltage	$V_{REF} = V_{DDQ}/2$	V_{DDQ}/2+300mV	-	-	V
V_{SL}	Low Swing Low-Level Input Voltage	$V_{REF} = V_{DDQ}/2$	-40	-	V_{DDQ}/2-100mV	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} =18m	-	-	GND –0.8	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} =18mA	-	-	VCC+0.8	V
I_{IL}	Input Leakage Current	-	-10	-	10	µA

Notes: [1] *Guaranteed by design.*
[2] *V_{DDQ} Defines max voltage level of low swing input. It is not actual input voltage.*

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AC Specifications

Under normal operating conditions unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIP}	IDCK Period, 1-pixel/clock	-	6.06	-	40	ns
F_{CIP}	IDCK Frequency, 1-pixel/clock	-	25	-	165	MHZ
T_{CIH}	IDCK High Time at 165MHZ	-	2.0	-	-	ns
T_{CIL}	IDCK Low Time at 165MHZ	-	2.0	-	-	ns
T_{IJIT}	Worst Case IDCK Clock Jitter[2,3]	-	-	-	2	ns
T_{SIDF}	Data, DE,VSYNC, HSYNC Setup Time to IDCK falling edge	Single Edge (DSEL = 0, DKEN = 0, EDGE = 0)	1.0	-	-	ns
T_{HIDF}	Data, DE,VSYNC, HSYNC Hold Time to IDCK falling edge	Single Edge (DSEL = 0, DKEN = 0, EDGE = 0)	0.9	-	-	ns
T_{SIDR}	Data, DE,VSYNC, HSYNC Setup time to IDCK rising edge[1]	Single Edge (DSEL = 1, DKEN = 0, EDGE = 1)	1.0	-	-	ns
T_{HIDR}	Data, DE,VSYNC, HSYNC Hold Time to IDCK rising edge[1]	Single Edge (DSEL = 1, DKEN = 0, EDGE = 1)	0.9	-	-	ns
T_{SID}	Data, DE,VSYNC, HSYNC Setup time to IDCK rising/falling edge[1]	Dual Edge (DSEL = 1, DKEN = 0, BSEL =0)	0.6	-	-	ns
T_{HID}	Data, DE,VSYNC, HSYNC Hold Time to IDCK rising/falling edge[1]	Dual Edge (DSEL = 1, DKEN = 0, BSEL =0)	1.3	-	-	ns
T_{DDF}	VSYNC,HSYNC Delay from DE falling edge[1]	-	1 T_{CIP}	-	-	ns
T_{DDR}	VSYNC,HSYNC Delay from DE rising edge[1]	-	1 T_{CIP}	-	-	ns
T_{HDE}	DE high time[1]	Vertical Blanking Only	-	-	819T_{CIP}	ns
T_{LDE}	DE low time[1,4]	Vertical Blanking Only	128T_{CIP}	-	-	ns
T_{STEP}	De-skew step size increment	DKEN = 1	-	260	-	ps
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5Pf, R_{LOAD} = 50Ω, $R_{EXT\ SWING}$ = 510Ω	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5Pf, R_{LOAD} = 50Ω, $R_{EXT\ SWING}$ = 510Ω	170	200	230	ps

Notes:
[1]Guaranteed by design.
[2]Jitter can be estimated by 1) triggering a digital scope at the rising of input clock and measuring the peak to peak time spread of the rising edge of the input clock at both 0.5µs and 1.0µs after the trigger.
[3]Actual jitter tolerance may be higher depending on the frequency of the jitter.
[4]DE Low time as defined as per DVI 1.0 Specification, Section 3.4 Link Timing Requirement.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage	$R_{LOAD} = 50\Omega$	-	-	-	-
	Single ended peak to peak amplitude	$R_{EXT\ SWING} = 510\Omega$	510	550	590	mV
V_{DDH}	Differential High-level Output Voltage	-	-	AVCC	-	V
V_{REF}	Input Reference Voltage	Low Swing High Swing	0.5	$V_{DDQ}/2$ VCC	0.9	V
I_{DOS}	Differential Output Short Circuit Current	$V_{OUT} = 0V$	-	-	5	µA
I_{PD}	Power-down Current[2]	25º C Ambient, $V_{CC} = 3.3V$	-	0.2	1.0	mA
I_{CCT}	Transmitter Supply Current	DCLK = 165MHZ, 1 pixel/clock mode, $R_{EXT\ SWING} = 510\Omega$	-	-	-	-
		Worst Case Pattern[3] 25º C Ambient	-	85	120	mA

Notes: [1] Guaranteed by design.
[2] Assumes all input to the transmitter are not toggling.
[3] Black and white checkerboard patterns, each checker is one pixel wide

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Input Timing Diagrams

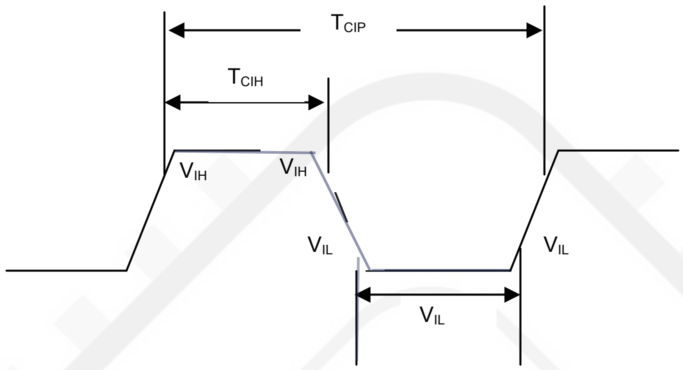

Figure 1. Clock Cycle/High/Low

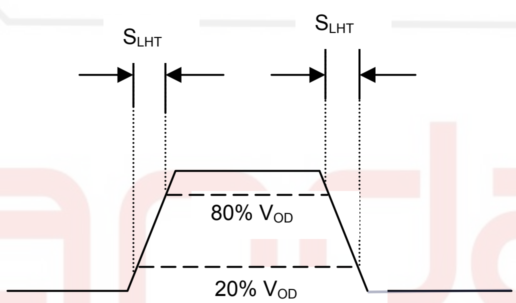

Figure 2. Differential Transition