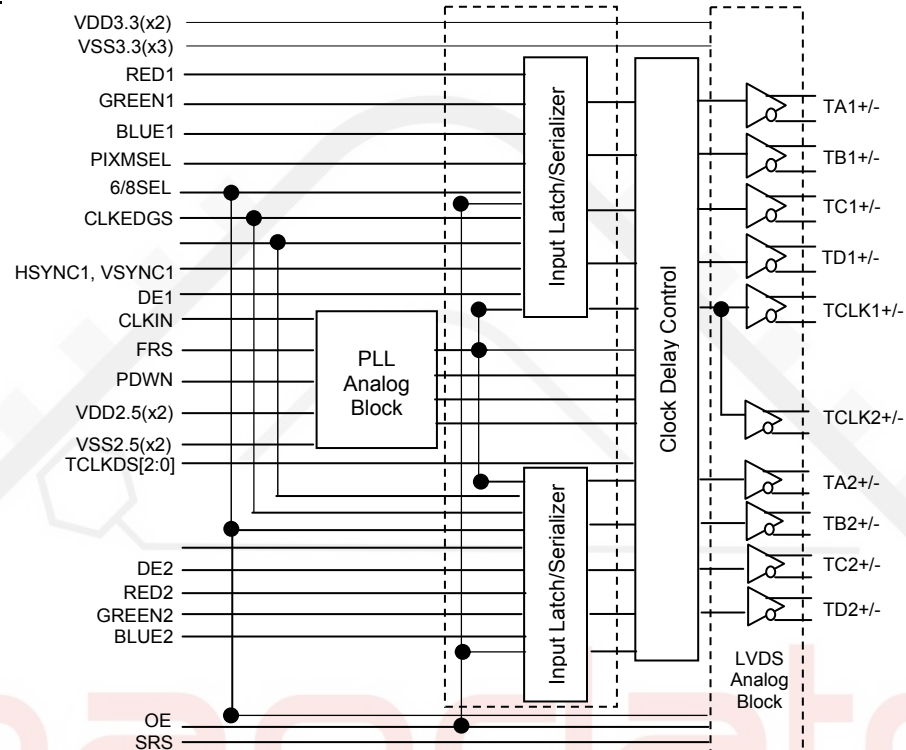


Block Diagram**Features**

- Input dot clock range: 25MHz~ 100MHz suited for VGA~UXGA
- Up to 5.6 Gbps bandwidth with dual link
- Clock edge selectable
- Supports both normal and reduced swing LVDS or low EMI
- 6/8 bits color selectable
- PLL requires no external components
- Power down mode
- Low Power consumption
- Compatible with IEEE 1596.3 LVDS standard
- Process Technology: 0.18um

Applications

Computer Display Devices, especially LCD or Flat-Panel based display

Description

LVDS Transmitter is designed to support Dual Link Transmission between Host and Flat Panel Display up to UXGA resolutions. The transmitter converts 48bits or 36bits of CMOS data into 8 LVDS data streams. It can be programmed for input data latching at either rising edge or falling edge clock through a dedicated pin. The output clock delay referring to data stream can also be configured by input pins, which eases the application in the receiving site.

LVDS are supported for low EMI. To minimize the EMI further, SSCG modulated clock input is also supported by the transmitter. In Dual Link, the transmit clock frequency of 100 MHz, 48bits of RGB data are transmitted at an effective rate of 700 Mbps per LVDS channel. This low voltage differential is what delivers higher data transmission speeds and inherently greater bandwidth at lower power consumption.